opposing sidewall surfaces, 106 and 108 respectively. A second gate 112 is located on, and opposes, a second one 108 of the opposing sidewall surfaces, 106 and 108 respectively. The threshold voltage (V_t) of the first gate 110 is dependent on the potential applied to the second gate 112.

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. The substitute claim set is intended to reflect amendment of previously pending claims 1, 3, 4, 9, 12, 13, and 22-30. The specific amendments to individual claims are detailed in the following marked up set of claims.

1. (Amended) A method of fabricating a transistor on a substrate, the method comprising:

forming a first source/drain region on the substrate;

vertically forming a body region on the first source/drain region as a fully depleted structure, wherein vertically forming the body region includes vertically growing an epitaxial layer, and wherein the body region includes opposing sidewall surfaces;

forming a second source/drain region on the body region;

forming a first gate on a first one of the opposing sidewall surfaces; and

forming a second gate on a second one of the opposing sidewall surfaces.

3. (Amended) The method of claim 1, wherein forming the body region includes forming the body region having a thickness of less than 0.2 microns [as a fully depleted structure].

4. (Amended) The method of claim 1, wherein forming the transistor includes forming the body region having a thickness of about 0.4 microns[, the first gate, and the second gate such that biasing the first and the second gates fully depletes the body region].

9. (Amended) A method of fabricating a transistor on a substrate, the method comprising:

forming a first conductivity type first source/drain region on the substrate;

vertically forming a second conductivity type body region on the first source/drain layer, wherein vertically forming the body region includes vertically growing an epitaxial layer as a fully depleted structure, and wherein the body region includes opposing sidewall surfaces;

forming a first conductivity type second source/drain region on the body region layer;

forming a first gate on a first one of the opposing sidewall surfaces; and

forming a second gate on a second one of the opposing sidewall surfaces.

12. (Amended) The method of claim 9, wherein vertically forming a second conductivity type body region includes forming [a fully depleted body region.] , wherein forming the second conductivity type body region having a thickness of less than 0.2 microns.

13. (Amended) A method of fabricating a transistor on a substrate, the method comprising:

vertically growing an n-type epitaxial first source/drain region on the substrate;

vertically forming a second conductivity type body region on the first source/drain layer as a fully depleted structure, wherein vertically forming the body region includes vertically growing an epitaxial layer, and wherein the body region includes opposing sidewall surfaces;

vertically growing an n-type epitaxial second source/drain region on the body region layer;

forming a first gate on a first one of the opposing sidewall surfaces; and

forming a second gate on a second one of the opposing sidewall surfaces.

22. (Amended) The method [dual-gated transistor] of claim 21, including fabricating the dual-gated transistor on a p-type bulk silicon substrate.

23. (Amended) The method [dual-gated transistor] of claim 21, including forming the body region, the first gate, and the second gate such that biasing the first and the second gates fully depletes the body region.

24. (Amended) The method [dual-gated transistor] of claim 21, including forming the first source/drain region using ion implantation.

25. (Amended) The method [dual-gated transistor] of claim 21, wherein forming the first source/drain region includes vertically growing an epitaxial layer.

26. (Amended) The method [dual-gated transistor] of claim 21, wherein forming the first source/drain region includes using ion implantation and includes vertically growing an epitaxial layer.

27. (Amended) The method [dual-gated transistor] of claim 21, including encasing a portion of the body region with Arsenic silicate glass (ASG) and annealing the ASG.

28. (Amended) The method [dual-gated transistor] of claim 27, including performing chemical vapor deposition (CVD) to deposit the ASG.

29. (Amended) The method [dual-gated transistor] of claim 21, wherein forming a first source/drain region adjacent to the body region includes encasing a portion of the body region with Borosilicate silicate glass (BSG) and includes annealing the BSG.

30. (Amended) The method [dual-gated transistor] of claim 32, including using chemical vapor deposition (CVD) to deposit the BSG.

REMARKS

Applicant has reviewed and considered the Office Action mailed on August 28, 2002, and the references cited therewith.

Claims 1, 3, 4, 8, 9, 12, 13, and 22-30 are amended and no claims are canceled; as a result, claims 1-30 are now pending in this application. The amendments are fully supported by